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(71) Applicants:
- **RAMTRON INTERNATIONAL CORPORATION**
  Colorado Springs, Colorado 80921 (US)
- **FUJITSU LIMITED**
  Kawasaki-shi, Kanagawa 211-8588 (JP)

(72) Inventors:
- **Argos, George**
  Colorado Springs, Colorado 80920 (US)
- **Yamazaki, Tatsuya**
  Kawasaki 214 (JP)

(74) Representative: **Burke, Steven David et al**
R.G.C. Jenkins & Co.
26 Caxton Street
London SW1H 0RJ (GB)

(54) Dual-level metalization method for integrated circuit ferroelectric devices

(57) A dual-level metalization method for ferroelectric integrated circuits includes the steps forming a planarized oxide layer over a partially formed integrated circuit ferroelectric device, forming a cap layer over the planarized oxide layer, forming vias into the planarized oxide layer and cap layer to provide access to the desired first-level metal contacts, and metalizing the selected first-level metal contacts with second-level metal. The cap layer can be doped or undoped titanates, zirconates, niobates, tantalates, stanates, hafnates, or manganates such as doped and undoped PZT (lead zirconate titanate), BST (barium strontium titanate), or SBT (strontium bismuth tantalate).

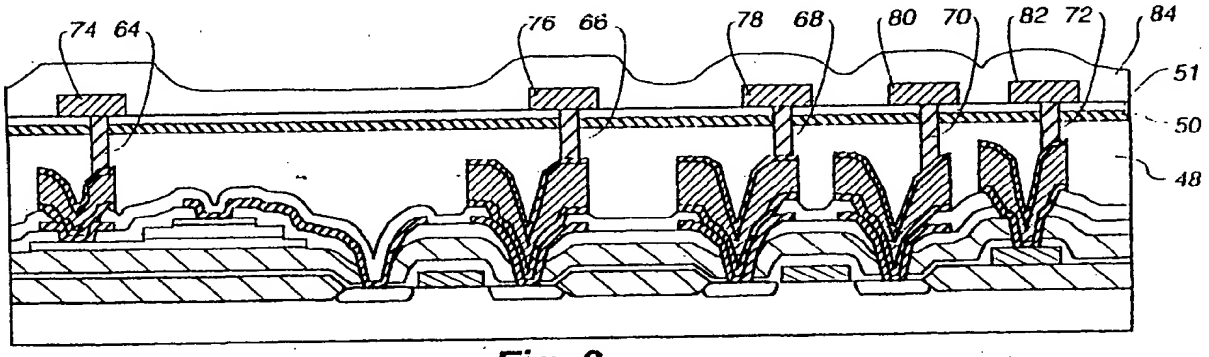

Fig. 8

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Description

FIELD OF THE INVENTION

This invention relates generally to integrated circuit ferroelectric devices such as ferroelectric capacitors, ferroelectric transistors, ferroelectric memory cells, and the like. More particularly, the present invention relates to a dual-level metalization fabrication method for preventing degradation in the electrical performance of ferroelectric capacitors and transistors.

BACKGROUND OF THE INVENTION

Dual-level or multi-level metalization schemes for integrated circuits are well known and have numerous advantages including smaller integrated circuit die size, increased device speed ease of design, as well as advantages related to the planarization of device topology.

One of the disadvantages of a multi-level metalization is the increased number of processing steps due to the deposition patterning and etching of the required additional metal oxide and passivation layers. While the additional processing steps are generally compatible with standard silicon based integrated circuits, the additional processing steps may adversely affect ferroelectric integrated circuit devices For example, hydrogen generated during any of the subsequent processing steps may adversely affect the integrity of the ferroelectric dielectric layer of a ferroelectric capacitor, resulting in degraded electrical performance.

What is desired, therefore, is a dual-level metalization method and structure that is compatible with a ferroelectric-based integrated circuit.

SUMMARY OF THE INVENTION

It is, therefore, a principal object of the present invention to provide a dual-level metalization fabrication method that retains the desirable characteristics of these metalization methods, yet is compatible with integrated circuit ferroelectric devices.

It is another object of the invention to improve the electrical switching performance of integrated circuit ferroelectric capacitors and transistors having a dual-level metalization by reducing sensitivity to hydrogen.

It is another object of the invention to improve the overall electrical performance of ferroelectric memory circuits.

It is an advantage of the invention that the fabrication method of the present invention is compatible with existing ferroelectric capacitor and ferroelectric memory fabrication methods.

It is another advantage of the invention that it permits the deposition, patterning, and etching of a dual-level metalization scheme on a ferroelectric-based integrated circuit ferroelectric without subsequent degradation to the electrical performance of the ferroelectric devices.

It is another advantage of the invention that the dual-level metalization method set forth herein can be used in a wide array of ferroelectric-based electronic products such as integrated circuit memories and other ferroelectric integrated circuits, as well as RF/ID integrated circuits and cards.

A first dual-level metalization method for ferroelectric integrated circuits according to the present invention includes the steps of partially forming an integrated circuit ferroelectric device having a plurality of first-level metal contacts, forming a planarized oxide layer over the integrated circuit ferroelectric device, forming a cap layer over the planarized oxide layer, forming vias into the planarized oxide layer and cap layer to provide access to selected first-level metal contacts, and metalizing the selected first-level metal contacts with second-level metal. The second-level metal typically includes tungsten plugs, as well as a second patterned aluminum metal layer.

Second and third alternative dual-level metalization method according to the present invention include the steps of etching vias into the planarized oxide layer first, and then subsequently depositing the cap layer so that the cap layer extends fully or partially along the sidewalls of the vias. Either sloped-sidewall or trench vias can be used. A fourth alternative dual-level metalization method includes the use of a partial cap layer that only selectively protects underlying ferroelectric layers from hydrogen damage.

The cap layer can be fabricated using doped or undoped titanates, zirconates, niobates, tantalates, stanates, hafnates, or manganates such as doped and undoped PZT (lead zirconate titanate), BST (barium strontium titanate), or SBT (strontium bismuth tantalate). The cap layer itself need not be ferroelectric, since the electrical switching performance of the cap layer is not actually used, only its ability to getter hydrogen and thus protect the underlying ferroelectric layers.

The foregoing and other objects, features and advantages of the invention will become more readily apparent from the following detailed description of a preferred embodiment of the invention which proceeds with reference to the accompanying drawings:

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1-8 are sequential cross-sectional views of an integrated circuit ferroelectric memory being fabricated with a dual-level metalization method according to a first method of the present invention;

FIGS. 9-16 are sequential cross-sectional views of an integrated circuit ferroelectric memory being fabricated with a dual-level metalization method according to a second method of the present invention;

FIGS. 12A-12F are cross-sectional views of a via associated with the second method of the present

invention illustrating alternative methods for forming the protective cap layer inside the via;
FIGS. 17-22 are sequential cross-sectional views of an integrated circuit ferroelectric memory being fabricated with a dual-level metalization method according to a third method of the present invention;
FIGS. 20A-20D are cross-sectional views of a via associated with the third method of the present invention illustrating alternative methods for forming the protective cap laver inside the via; and
FIGS. 23-28 are sequential cross-sectional views of an integrated circuit ferroelectric memory being fabricated with a dual-level metalization method according to a fourth method of the present invention.

DETAILED DESCRIPTION

Referring now to FIG. 1, a portion of a partially fabricated integrated circuit ferroelectric memory includes: a silicon or other substrate 10; source/drain regions 12 and 14, as well a gate structure 22 (thin gate oxide and gate, shown undifferentiated in FIG. 1) for a first memory cell transistor; source/drain regions 16 and 18, as well as a gate structure 24 for a second memory cell transistor: a thick field oxide layer 20 for electrically isolating the transistors; a thin oxide layer 26; a BPSG oxide laver 28: a titanium/platinum bottom ferroelectric capacitor electrode 30; a ferroelectric dielectric layer 32 such as PZT or the like; a platinum top ferroelectric capacitor electrode 34; interlevel oxide layer 36; a local interconnect layer 38; a patterned titanium barrier laver 40; a patterned aluminum/silicon/copper first-level metalization layer 42; an oxide layer 44; and a patterned titanium nitride layer 46. Five first-level metal contacts 45 are shown in FIG. 1, which include patterned metal layers 42, 44, and 46. The partially fabricated integrated circuit ferroelectric memory of FIG. 1 is but one example of a ferroelectric device or structure having a first-level metalization scheme that can use the dual-level metalization method of the present invention. Any other integrated circuit ferroelectric device or structure can be used as the starting point for the dual-level metalization method of the present invention.

In FIG. 2 an oxide layer 48 is formed over the integrated circuit ferroelectric device by plasma depositing or spin-on to a conformal thickness of about 10,000 to 20,000 Angstroms (10 to 20 μm). Oxide layer 48 is planarized to a maximum thickness of about 5,000 Angstroms (5 μm) by chemical-mechanical polishing (CMP). Also shown in FIG. 2, a cap layer 50 is formed over the planarized oxide layer 48 by either sputtering, sol-gel, or other techniques to a thickness of about 200 to 10,000 Angstroms. Cap layer 50 can be formed of doped and undoped titanates, zirconates, niobates, tantalates, stanates, hafnates, and manganates. Cap layer 50 can either be ferroelectric or non-ferroelectric. Cap layer 50 is selected primarily for its ability to absorb hydrogen and to protect the ferroelectric dielectric layer 32 from degradation due to the stress of subsequent processing steps and not for its own electrical switching properties. Cap layer 50 can be formed of doped or undoped PZT, BST, or SBT, which may or may not be the same material selected for dielectric layer 32. Cap layer 50 and dielectric layer 32 may be the same, for example, if only one ferroelectric sputtering target is desired. Cap layer 50 and dielectric layer 32 may be different, for example, if a lower-cost target or method of forming cap layer 50 is desired. Once cap layer 50 has been formed, it may be stabilized if desired with an optional heat treatment. The time and temperature of the heat treatment will vary with the type of material selected for cap layer 50.

In FIG. 3 an optional oxide layer 51 is formed over cap layer 50 to a thickness of between 500 and 5000 Angstroms. Oxide layer 51 may be used to prevent potential problems related to the direct contact of cap layer 50 with the subsequent second-level metal materials, such as aluminum.

In FIG. 4 vias 52, 54, 56, 58, and 60 are formed into the planarized oxide layer 48, cap layer 50, and optional oxide layer 51 to provide access to selected first-level metal contacts 45. In FIG. 3, access is made to all of the first-level metal contacts 45. This is an example only, and access can be made to the first-level metal contact or not made as required for a given application. Etching is typically accomplished by a reactive-ion etch (RIE). While the RIE etch will be tailored to the specific cap layer 50 and planarized oxide layer 48 as required, a desirable RIE etch includes a gas mixture of CHF_3, C_2F_6, and helium energized to 700 Watts in a vacuum of about 1900 mTorr.

In FIG. 5, the selected first-level metal contacts are initially metalized with a tungsten layer 62, including the pre-deposition of a thin TiN nucleation layer, typically 100 to 1000 Angstroms thick. The thin TiN nucleation layer is used to ensure the proper adhesion of the tungsten layer 62. Tungsten layer 62 is formed to a thickness of about 5,000 Angstroms, but at a minimum should be of sufficient thickness to completely fill previously formed vias 52-60. If desired, layer 62 can also be formed of copper or aluminum, as well as alloys of these metals.

In FIG. 6, the tungsten layer 62 is removed by CMP except for the tungsten plugs 64, 66, 68, 70, and 72 remaining in vias 52-60.

In FIG. 7, tungsten plugs 64-72 are metalized with a second layer of metal. Patterned metal areas 74, 76, 78, 80, and 82 are shown in electrical contact with tungsten plugs 64-72. The metal used to form metal areas 74-82 can be aluminum or an alloy of aluminum and copper, or an alloy of aluminum, copper, and silicon, or other conventional metalization layers as desired. Metal areas 74-82 and metal plugs 64-72 together form the second-level metal for the method of the present invention.

In FIG. 8, the integrated circuit is passivated with passivation layer 84. Passivation laver 84 can be a conventional passivation layer such as SiO_2 or Si_3N_4, or the

like, or a passivation layer as described in US Patents 5,578,867 and 5,438,023, both of which are assigned to the assignee of the present application, and both of which are hereby incorporated by reference.

Figure 9 is identical to FIG. 1, and serves as the starting point for the second method of the present invention. An integrated circuit ferroelectric device is shown having five first-level metal contacts 46. The same number designations are used for the same layers as were used in FIGS. 1-8.

In FIG. 10, a planarized oxide layer 48 is formed over the integrated circuit ferroelectric device. After oxide layer 48 is formed and planarized, vias 52-60 having sloped sidewalls are etched into the planarized oxide layer 48 to provide access to selected first-level metal contacts 45. The angle of the sidewall slope is used to facilitate the subsequent deposition of cap layer 50 and optional oxide layer 51. The sloping sidewalls may be etched by conventional means such as wet chemical etching or an isotropic reactive-ion etch (RIE).

In FIG. 11, cap layer 50 and optional oxide layer 51 are formed over the planarized oxide layer 48 and vias 52-60. Cap layer 50 and optional oxide layer 51 conformally coat the surface of cap layer 50 and the sidewalls and bottom portion of vias 52-60.

In FIG. 12, the bottom portion of vias 52-60 are etched to provide access to first level contacts 45. While vias 52-60 may be further etched exactly as shown in FIG. 12, numerous variations exist for the etching of cap layer 50 and optional oxide layer 51. Some of these variations are shown in further detail in FIGS. 12A-12F.

In FIG. 12A, only the optional oxide layer 51 is etched at the bottom portion of the via. Cap layer 50 is left unetched at the bottom of the via. Depending on the thickness of cap layer 50 and the resistivity of this layer, it may be acceptable, if desired, to leave the cap layer unetched. In other words, the remaining portion of cap layer 50 may not significantly increase the series resistance of the subsequently formed metal plug. In FIG. 12B, cap layer 50 has been deposited first and etched beyond the immediate area of the bottom of the via. Optional oxide layer 51 has been subsequently deposited and etched to the dimensions of the bottom of the via, thereby overlapping and sealing cap layer 50. In FIG. 12C, both the cap layer 50 and the optional oxide layer 51 have been etched at the top of the via, which is similar to the profile shown in FIG. 4, except for the sloping sidewalls of the via. In FIG. 12D, cap layer 50 has been deposited first and etched at the top of the via. Optional oxide layer 51 has been subsequently deposited and etched to the dimensions of the bottom of the via, thereby overlapping cap layer 50. Figure 12E shows the cross-section of the via in which only the unetched cap layer 50 is present, and FIG. 12F shows the cross-section of the via in which only cap layer 50 is present, and etched corresponding to the dimensions of the bottom of the via.

The selected first-level metal contacts 45 are metalized with second-level metal and passivated in FIGS. 13-16, and correspond to previously described FIGS. 5-8. In FIG. 13, a tungsten or other metal layer 62 is formed, and in FIG. 14 the upper portion of layer 62 is removed to form metal plugs 64-72. In FIG. 15, the metal plugs are metalized with patterned second-level metal portions 74-82. In FIG. 16, the entire surface of the integrated circuit is passivated with passivation layer 84.

Figure 17 is again identical to FIG. 1, and serves as the starting point for the third method of the present invention. An integrated circuit ferroelectric device is shown having five first-level metal contacts 45. The same number designations are used for the same layers as were used in FIGS. 1-8, although the exact shapes of the layers may be altered.

In FIG. 18, a planarized oxide layer 48 is formed over the integrated circuit ferroelectric device. After oxide layer 48 is formed and planarized, trench vias 52-60 are etched into the planarized oxide layer 48 to provide access to selected first-level metal contacts 45. The trench vias may have the benefit of providing tighter packing density on the integrated circuit. The trench vias may be etched by conventional means such as a reactive-ion etch (RIE).

Figure 19 corresponds to previous FIG. 11, in which cap layer 50 and optional oxide layer 51 are formed over the planarized oxide layer 48 and trench vias 52-60. Cap layer 50 and optional oxide layer 51 conformally coat the surface of cap layer 50 and the sidewalls and bottom portion of vias 52-60. It may be necessary to adjust the thicknesses of cap layer 50 and optional oxide layer 50 to enable a conformal coating of the steep sidewalls of trench vias 52-60

Figure 20 corresponds to previous FIG. 12, in which the bottom portion of vias 52-60 are etched to provide access to first level contacts 45. While vias 52-60 may be further etched exactly as shown in FIG. 12, numerous variations exist for the etching of cap layer 50 and optional oxide layer 51. Some of these variations are shown in FIGS. 20A-20D.

In FIG. 20A, only the optional oxide layer 51 is etched at the bottom portion of the via. Cap layer 50 is left unetched at the bottom of the via. Depending on the thickness of cap layer 50 and the resistivity of this layer, it may be acceptable, if desired, to leave the cap layer unetched. In other words, the remaining portion of cap layer 50 may not significantly increased the series resistance of the subsequently formed metal plug. In FIG. 20B, cap layer 50 has been deposited first and etched at the top of the via. Optional oxide layer 51 has been subsequently deposited and etched to the dimensions of the bottom of the via, thereby overlapping and sealing cap layer 50. Figure 20C shows the cross-section of the via in which only the unetched cap layer 50 is present, and FIG. 20D shows the cross-section of the via in which cap layer 50 is etched to the dimensions of the bottom of the via.

The selected first-level metal contacts 45 are met-

alized with second-level metal and passivated in FIGS. 21-22, and these two figures correspond to the previous four drawings of FIGS. 5-8.

A fourth method for fabricating a two-level metal for a ferroelectric integrated circuit is shown in FIGS. 23-28. Again, the same numbers are used for the same layers as in previous drawing figures. In FIG. 23, the starting drawing figure is reproduced showing an integrated circuit ferroelectric device such as a memory, in which five first-level metal contacts 45 are shown. In FIG. 24, a cap layer is deposited and etched to form a partial cap layer 86. The partial cap layer 86 is etched to the approximate dimensions, or slightly overlapping, the dimensions of the ferroelectric layer 32 used in the integrated circuit. In FIGS. 23-28, ferroelectric layer 32 is a ferroelectric dielectric layer for a capacitor, but other ferroelectric layers can be similarly protected by partial cap layer 86. If desired, partial cap layer 86 can be patterned in a different manner than that shown in FIG. 24. For example, the dimensions of cap layer 86 can be extended laterally. It is recommended, however, that the cap layer be patterned so that it does not contact any of the first-level metal structures, which usually contain aluminum and other metals not compatible with the type of ceramic materials used for cap layer 86. In FIG. 25, an oxide layer 48 is deposited and planarized, and trench vias 52-60 are etched to the first-level metal contacts in FIG. 26. In FIG. 27, metal plugs 64-72 are formed. In FIG. 28, the metal plugs are metalized with a second-level patterned metal layer, and the entire integrated circuit is passivated.

Having described and illustrated the principles of the invention in a preferred embodiment thereof, it is appreciated by those having skill in the art that the invention can be modified in arrangement and detail without departing from such principles. For example, the following aspects of the semiconductor processes described herein can be changed as required: the types of dielectric materials; the thicknesses of the various layers; the types of ferroelectric materials; the etching processes; the electrode materials; and the exact via profile including the cap layer. Also, the specific application of the dual-level metalization method of the present invention is not limited to integrated circuit ferroelectric memory cells, although it is ideally suited to that application. We therefore claim all modifications and variation coming within the spirit and scope of the following claims.

Claims

1. A fabrication method comprising the steps of:

   forming an integrated circuit ferroelectric device having a plurality of first-level metal contacts;
   forming a planarized oxide layer over the integrated circuit ferroelectric device;
   forming a cap layer over the planarized oxide layer;
   forming vias into the planarized oxide layer and cap layer to provide access to selected first-level metal contacts; and
   metalizing the selected first-level metal contacts with second-level metal.

2. The fabrication method of claim 1 further comprising the step of forming an oxide layer over the cap layer before the vias are formed.

3. The fabrication method of claim 1 in which the step of forming a cap layer comprises the step of forming a layer of material selected from a group consisting of doped and undoped nitrides, titanates, zirconates, niobates, tantalates, stanates, hafnates, and manganates.

4. The fabrication method of claim 1 in which the step of forming a cap layer comprises the step of forming a layer of material selected from a group consisting of doped and undoped PZT, BST, and SBT.

5. A fabrication method comprising the steps of:

   forming an integrated circuit ferroelectric device having a plurality of first-level metal contacts;
   forming a planarized oxide layer over the integrated circuit ferroelectric device;
   forming vias into the planarized oxide layer to provide access to selected first-level metal contacts;
   forming a cap layer over the planarized oxide layer and vias; and
   metalizing the selected first-level metal contacts with second-level metal.

6. The fabrication method of claim 5 in which the step of forming vias comprises the step of forming a via having sloped sidewalls.

7. The fabrication method of claim 5 in which the step of forming vias comprises the step of forming trench vias.

8. The fabrication method of claim 5 further comprising the step of forming an oxide layer over the cap layer.

9. The fabrication method of claim 5 further comprising the step of etching a portion of the cap layer in the vias.

10. The fabrication method of claim 5 in which the step of forming a cap layer comprises the step of forming a layer of material selected from a group consisting

of doped and undoped nitrides, titanates, zirconates, niobates, tantalates, stanates, hafnates, and manganates.

11. The fabrication method of claim 5 in which the step of forming a cap laver comprises the step of forming a laver of material selected from a group consisting of doped and undoped PZT, BST, and SBT.

12. A fabrication method comprising the steps of:

forming an integrated circuit ferroelectric device having a plurality of first-level metal contacts;
forming a patterned cap layer over selected portions of the integrated circuit ferroelectric device including ferroelectric layers;
forming a planarized oxide layer over the integrated circuit ferroelectric device and patterned cap layer;
forming vias into the planarized oxide layer to provide access to selected first-level metal contacts; and
metalizing the selected first-level metal contacts with second-level metal.

13. The fabrication method of claim 1 in which the step of forming a patterned cap layer comprises the step of forming a layer of material selected from a group consisting of doped and undoped nitrides, titanates, zirconates, niobates, tantalates, stanates, hafnates, and manganates.

14. The fabrication method of claim 1 in which the step of forming a cap layer comprises the step of forming a layer of material selected from a group consisting of doped and undoped PZT, BST, and SBT.

15. A method of forming a dual-layer metalization for an integrated circuit comprising the steps of:

forming a hydrogen-resistant cap layer between first-level and second-level metal layers on the integrated circuit; and
electrically connecting the first-level and second-level metal layers with metal plugs extending through the cap layer.

16. The method of claim 15 in which the step of forming a hydrogen-resistant cap layer comprises the step of forming a laver of material selected from a group consisting of doped and undoped nitrides, titanates, zirconates, niobates, tantalates, stanates, hafnates, and manganates.

17. The fabrication method of claim 15 in which the step of forming a cap laver comprises the step of forming a laver of material selected from a group consisting of doped and undoped PZT, BST, and SBT.

18. A method of forming a dual-layer metalization for an integrated circuit comprising the steps of:

forming first-level metal contacts on the integrated circuit;
forming a patterned a hydrogen-resistant cap layer on selected portions of the integrated circuit;
electrically connecting the first-level and second-level metal layers with metal plugs extending through an oxide layer.

19. The method of claim 18 in which the step of forming a hydrogen-resistant cap layer comprises the step of forming a layer of material selected from a group consisting of doped and undoped nitrides, titanates, zirconates, niobates, tantalates, stanates, hainates, and manganates.

20. The fabrication method of claim 18 in which the step of forming a cap layer comprises the step of forming a layer of material selected from a group consisting of doped and undoped PZT, BST, and SBT.

21. A fabrication method comprising providing an integrated circuit ferroelectric device having a plurality of first-level metal contacts, forming second-level metalization contacting the first-level metal contacts through vias in a dielectric layer formed over the ferroelectric device, and forming a cap layer for protecting a ferroelectric layer within the ferroelectric device.

22. A ferroelectric device comprising a plurality of first-level metal contacts, second-level metalization contacting the first-level contacts through vias in a dielectric layer formed over the ferroelectric device, and a cap layer for protecting a ferroelectric layer within the ferroelectric device.

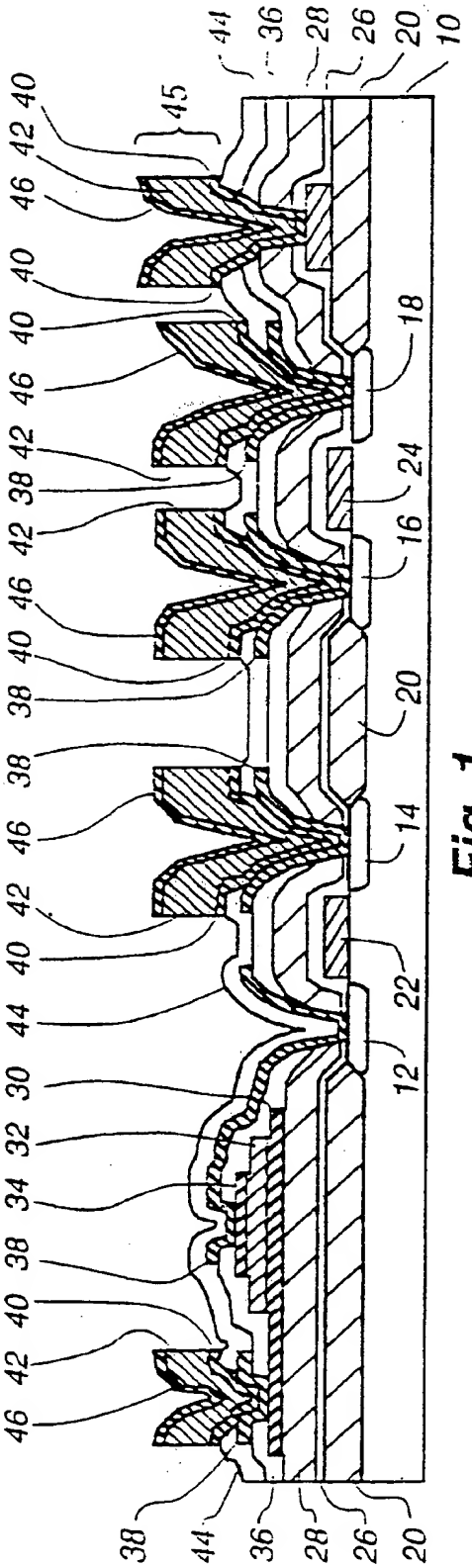

Fig. 1

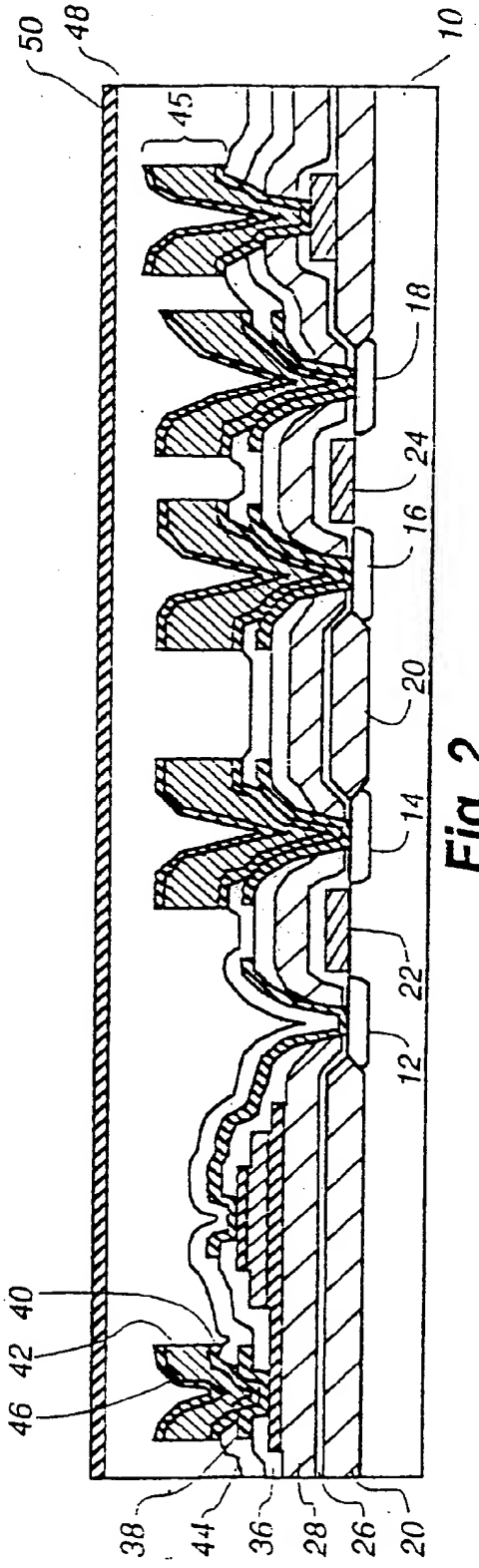

Fig. 2

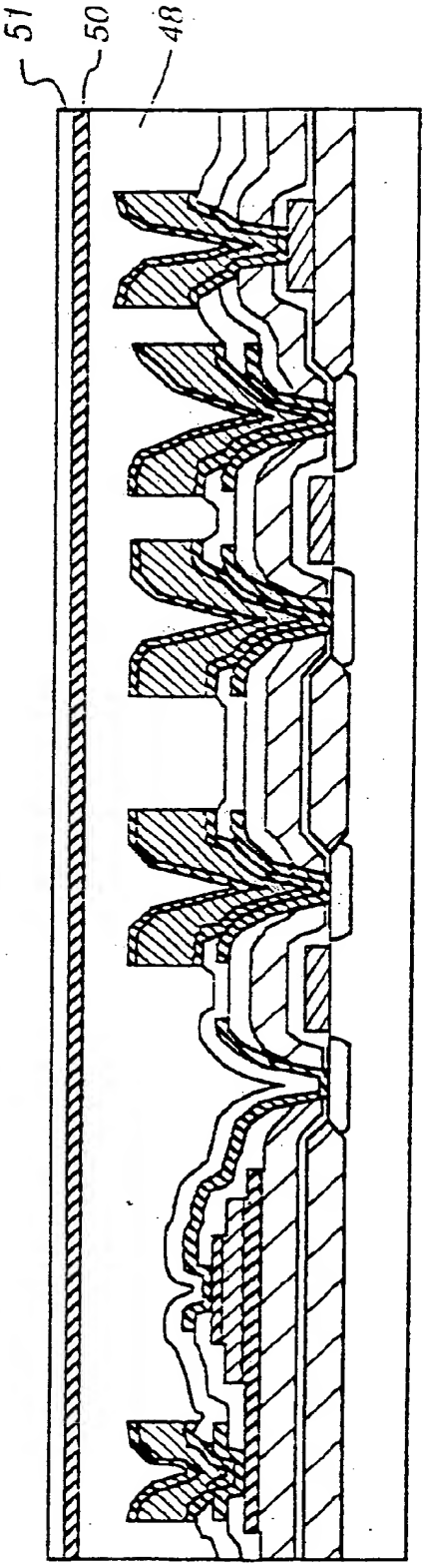

Fig. 3

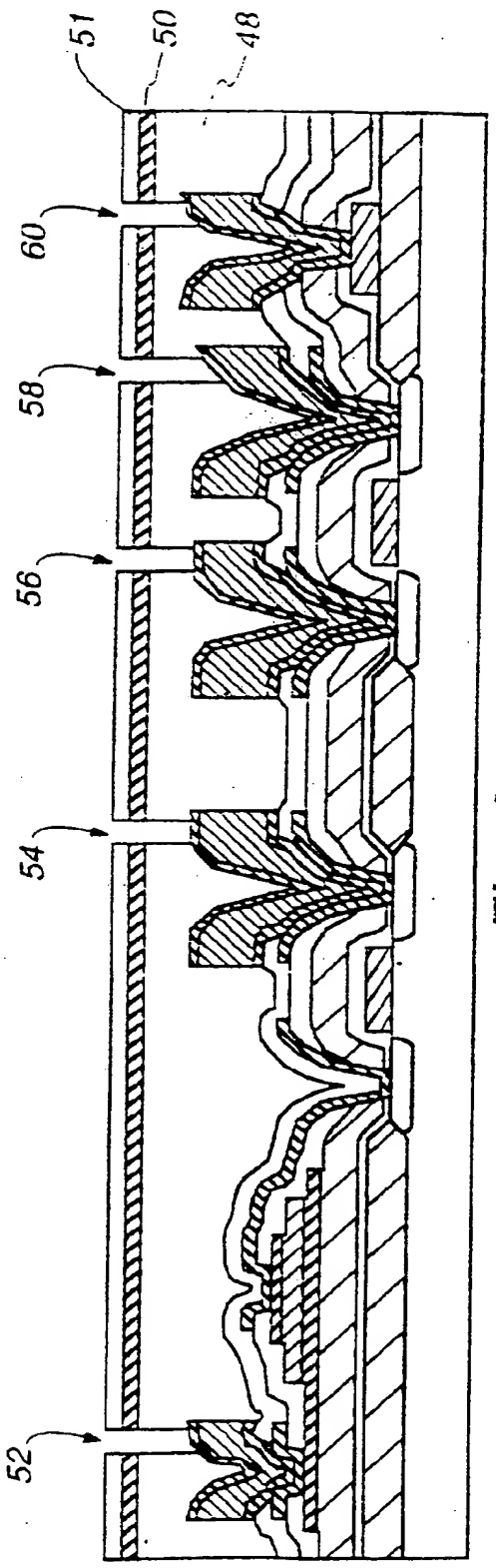

Fig. 4

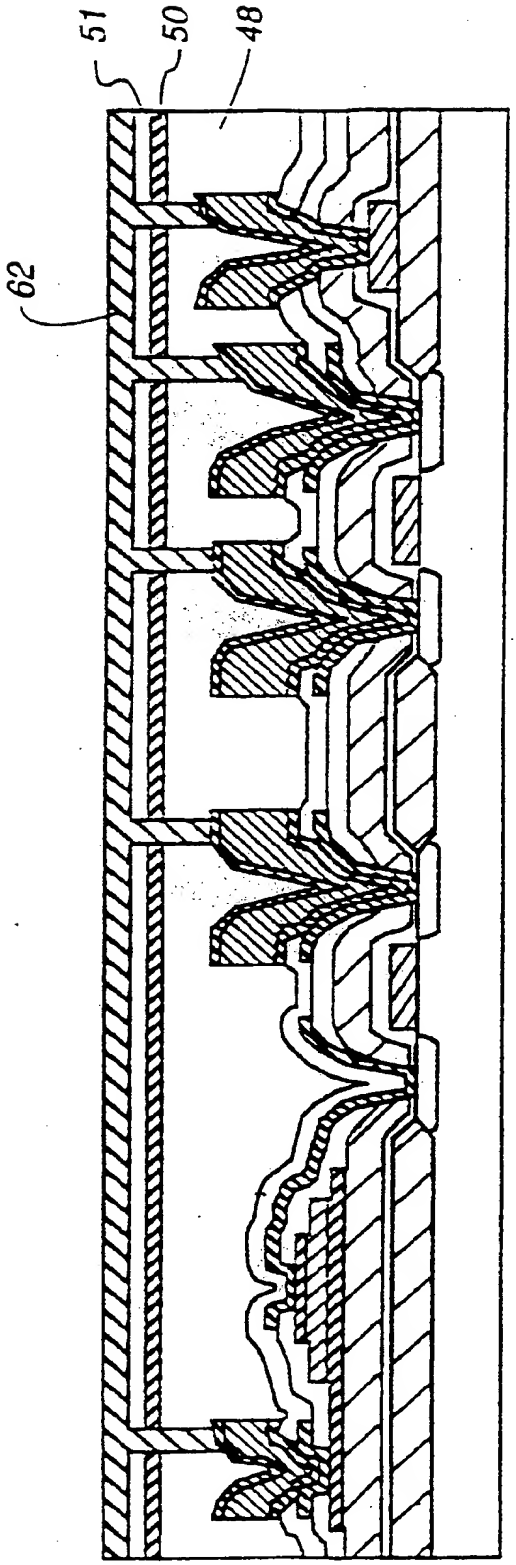

Fig. 5

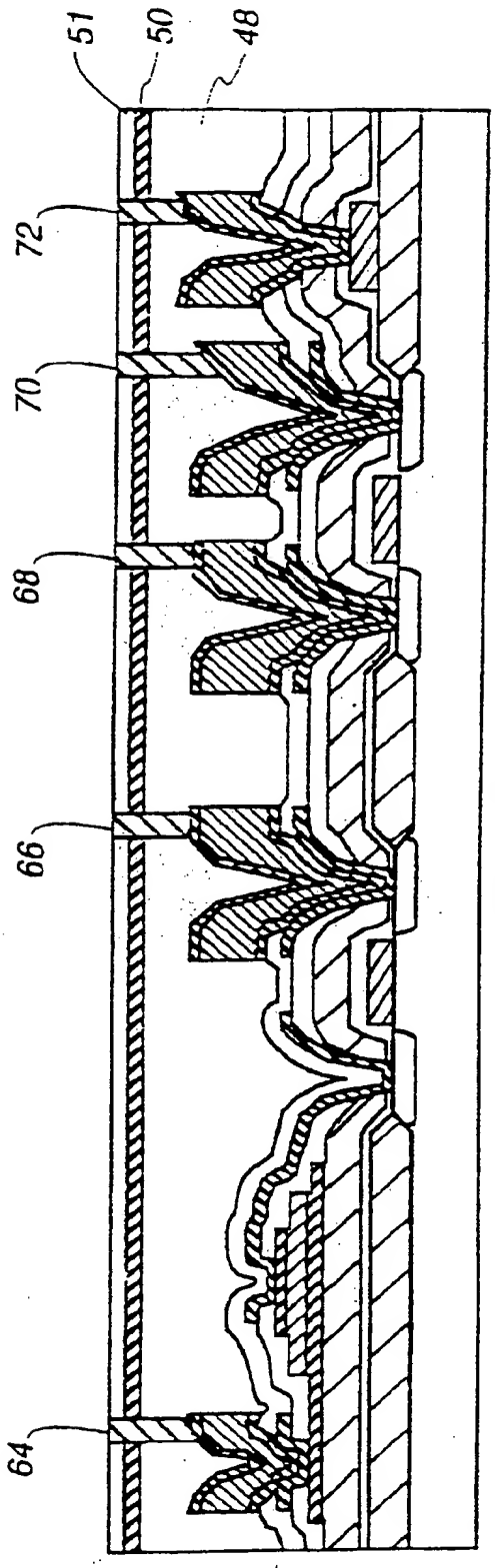

Fig. 6

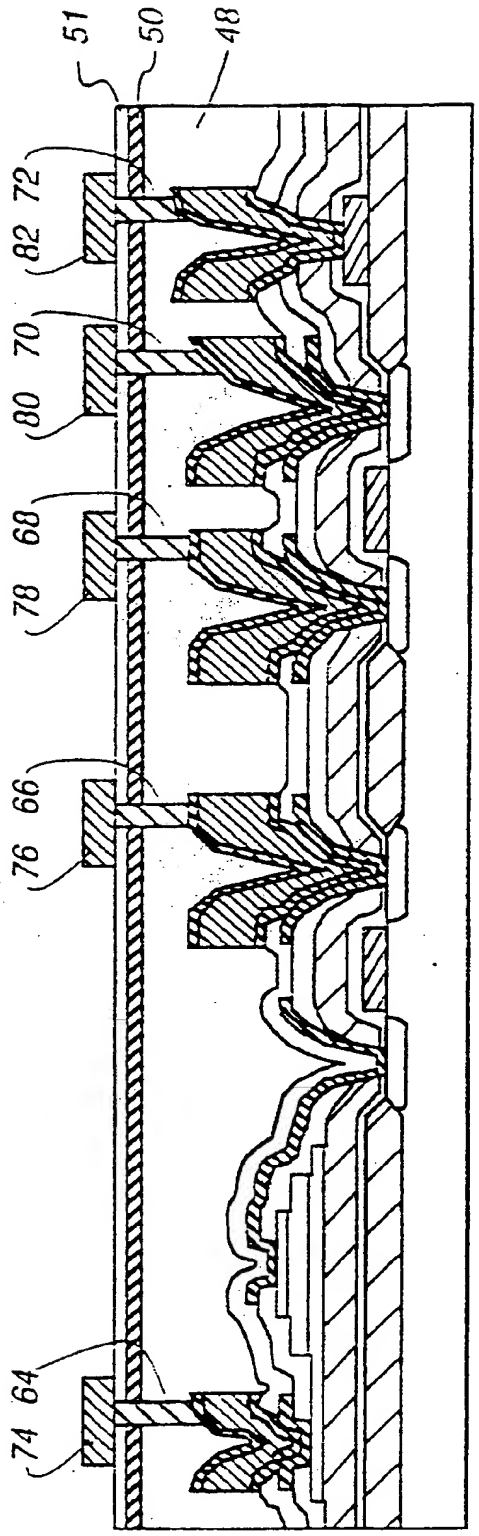

Fig. 7

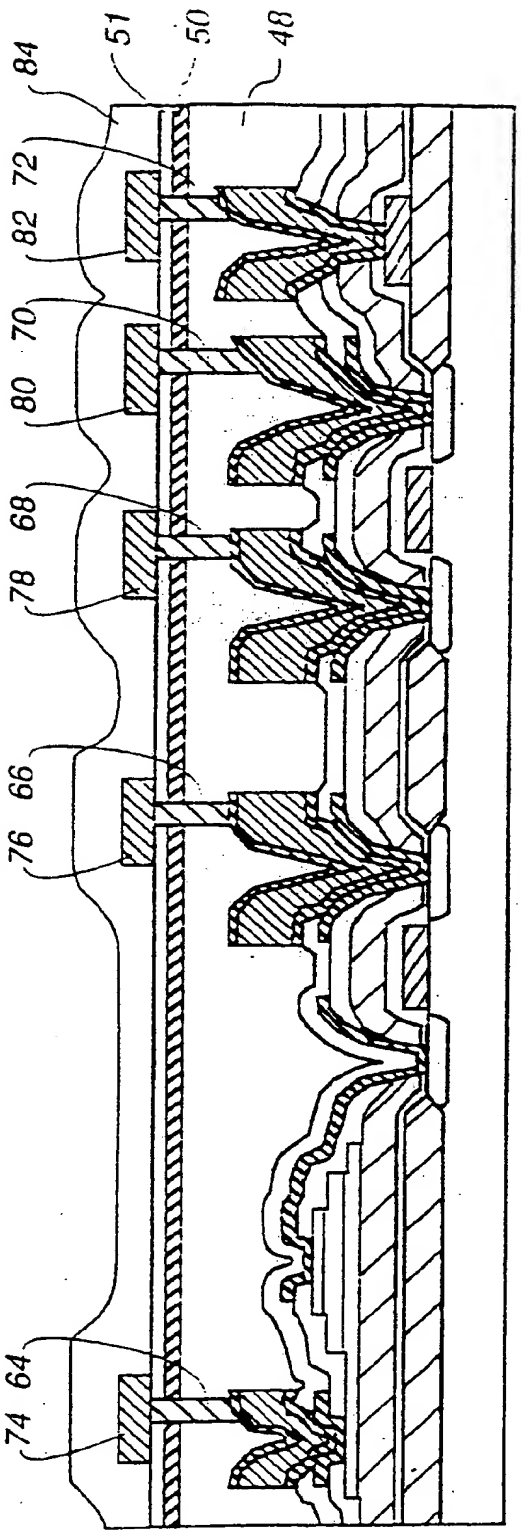

Fig. 8

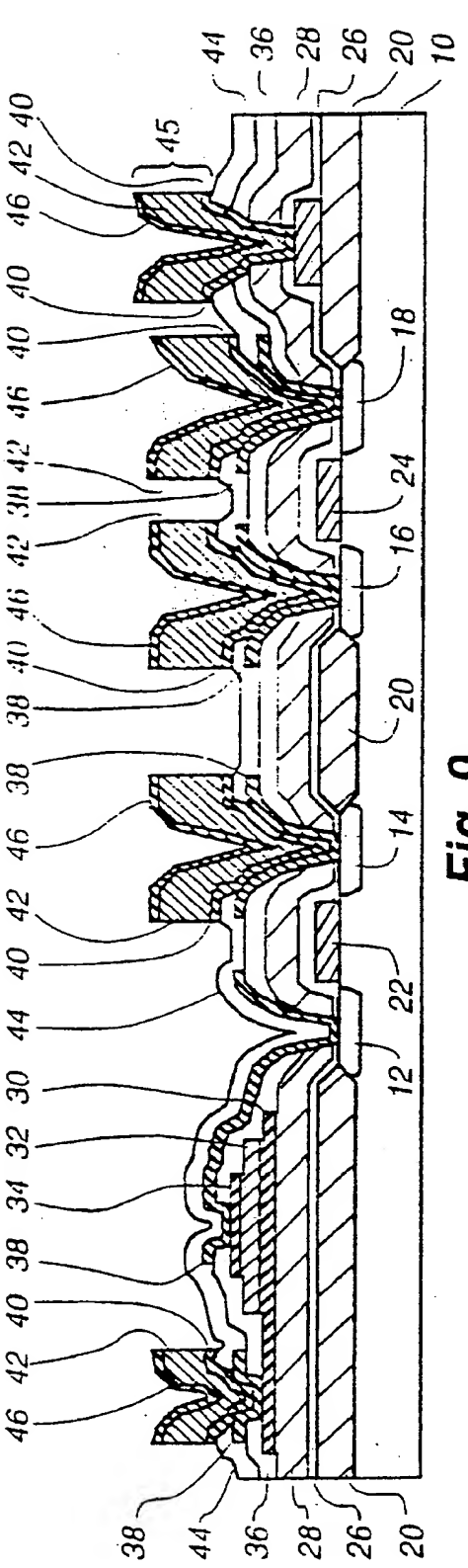
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Fig. 9

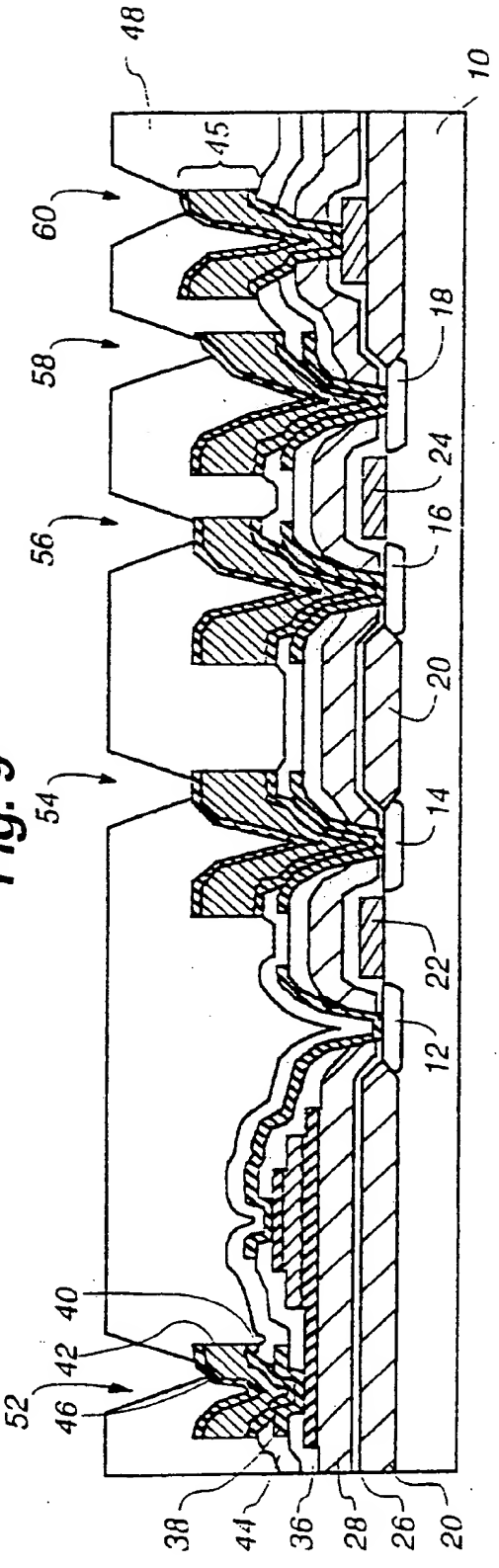
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Fig. 10

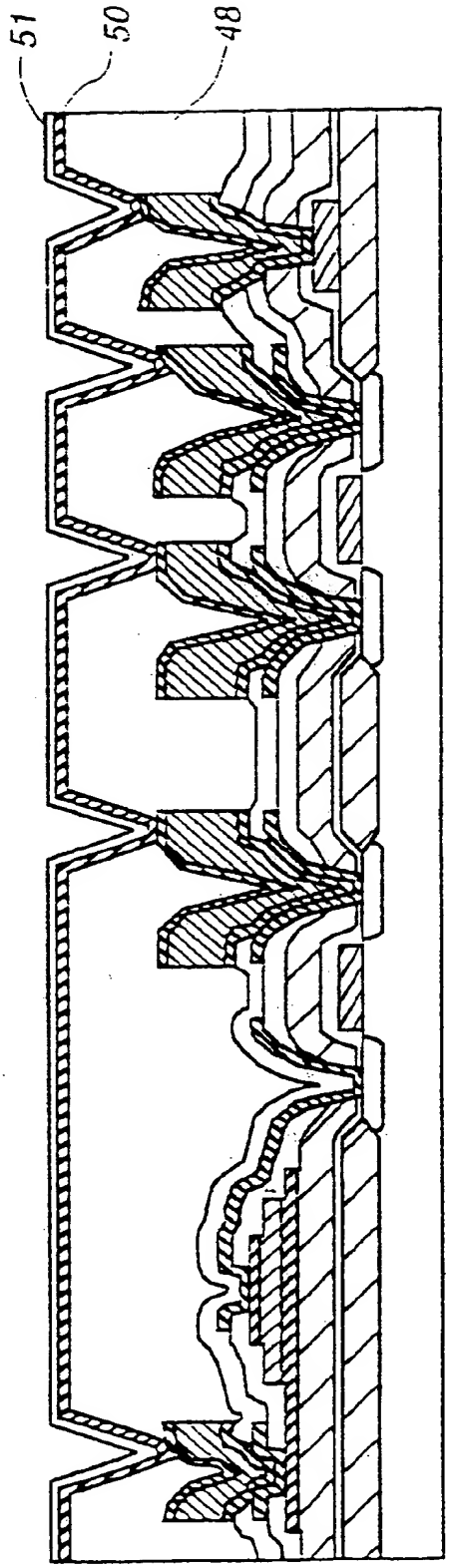


Fig. 11

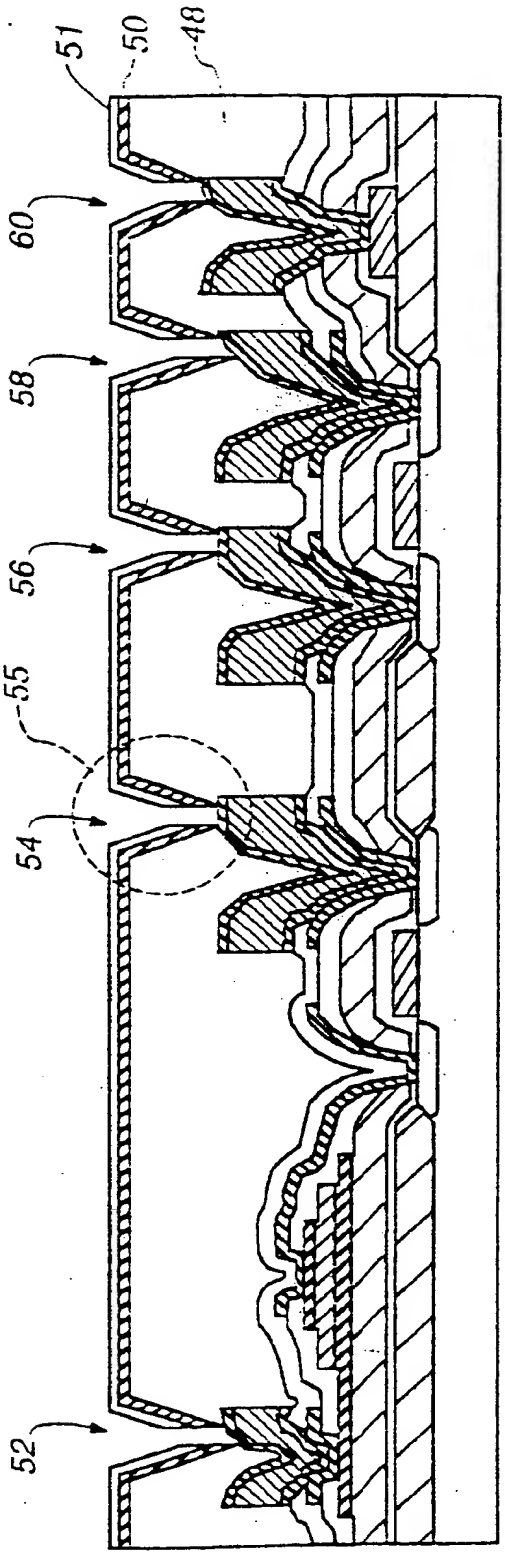


Fig. 12

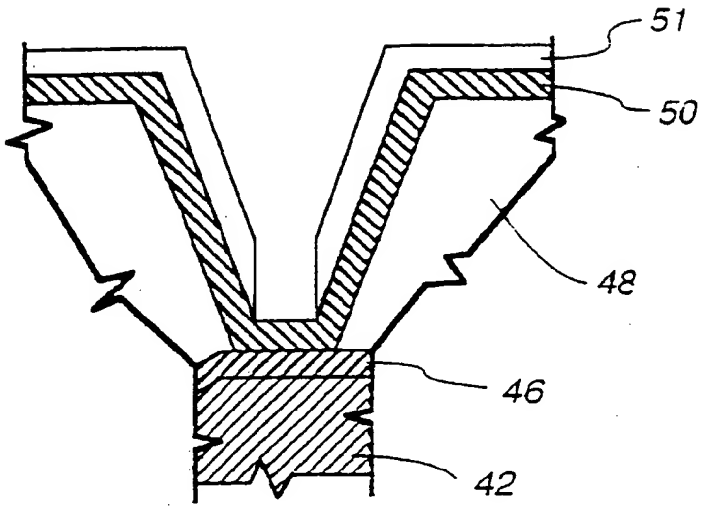


Fig. 12A

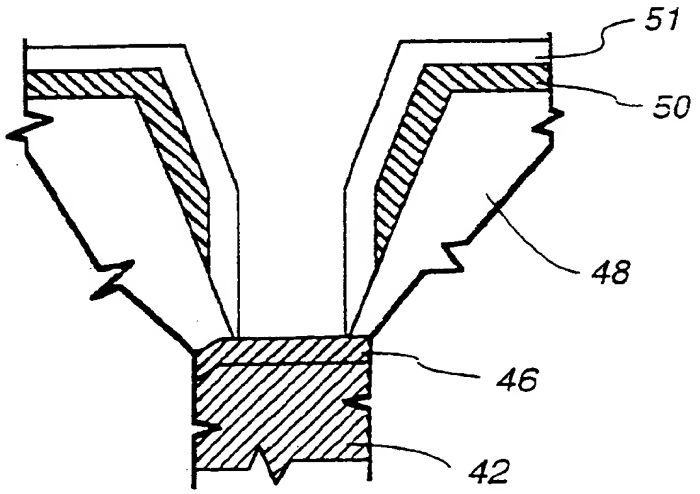


Fig. 12B

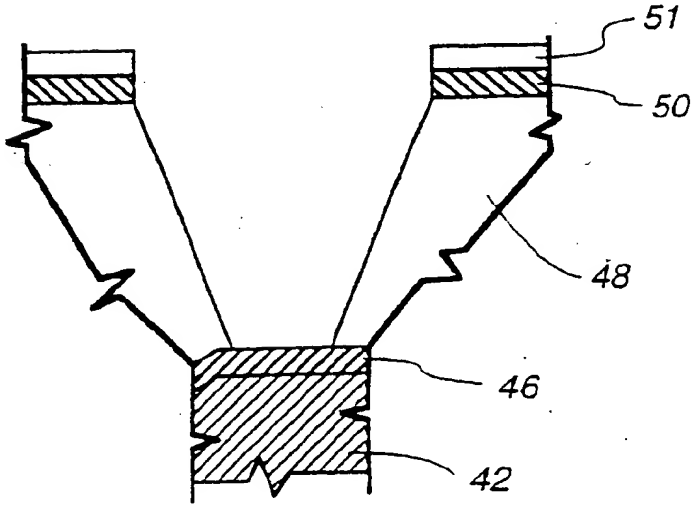


Fig. 12C

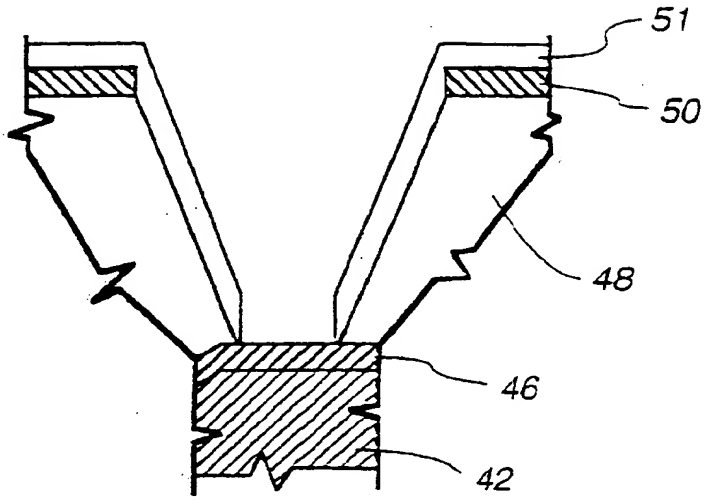


Fig. 12D

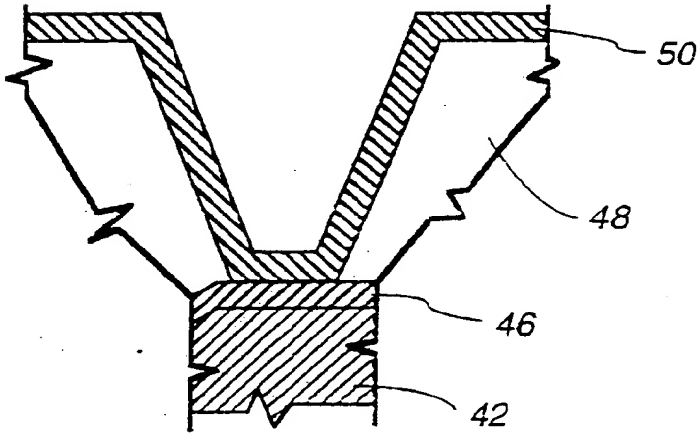


Fig. 12E

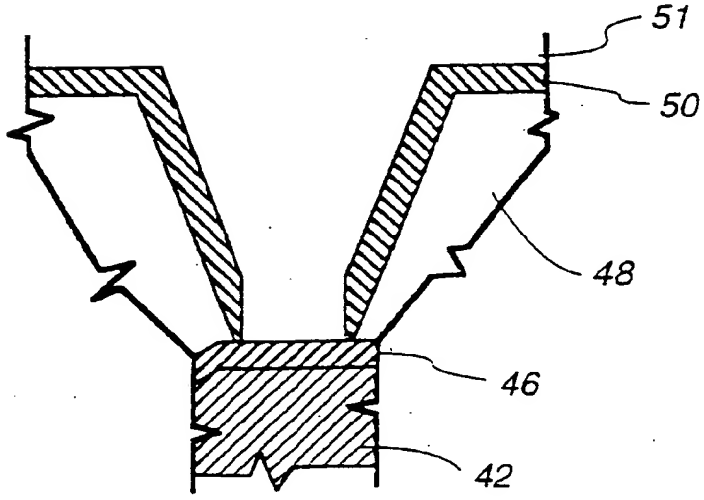
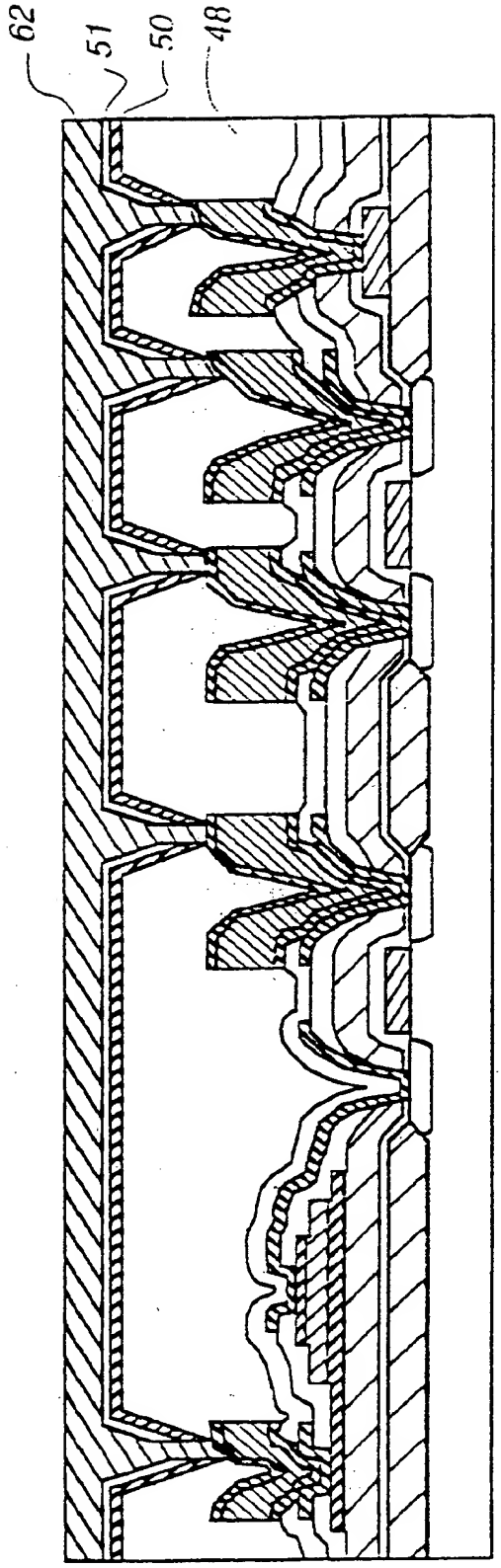


Fig. 12F



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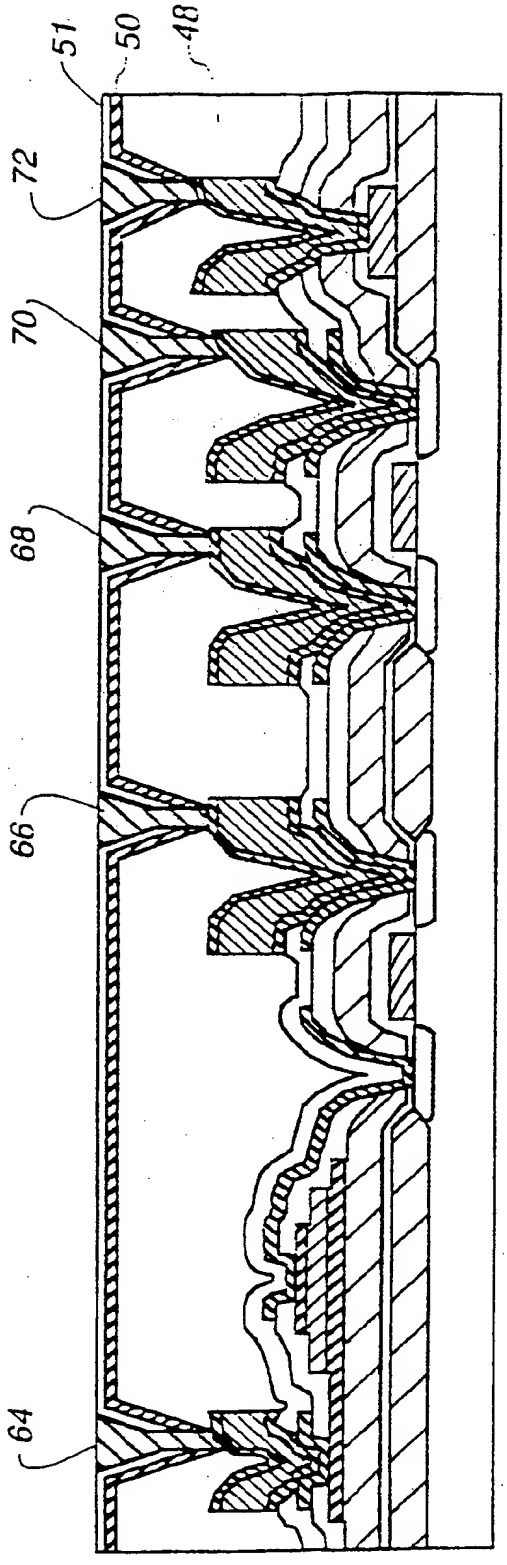

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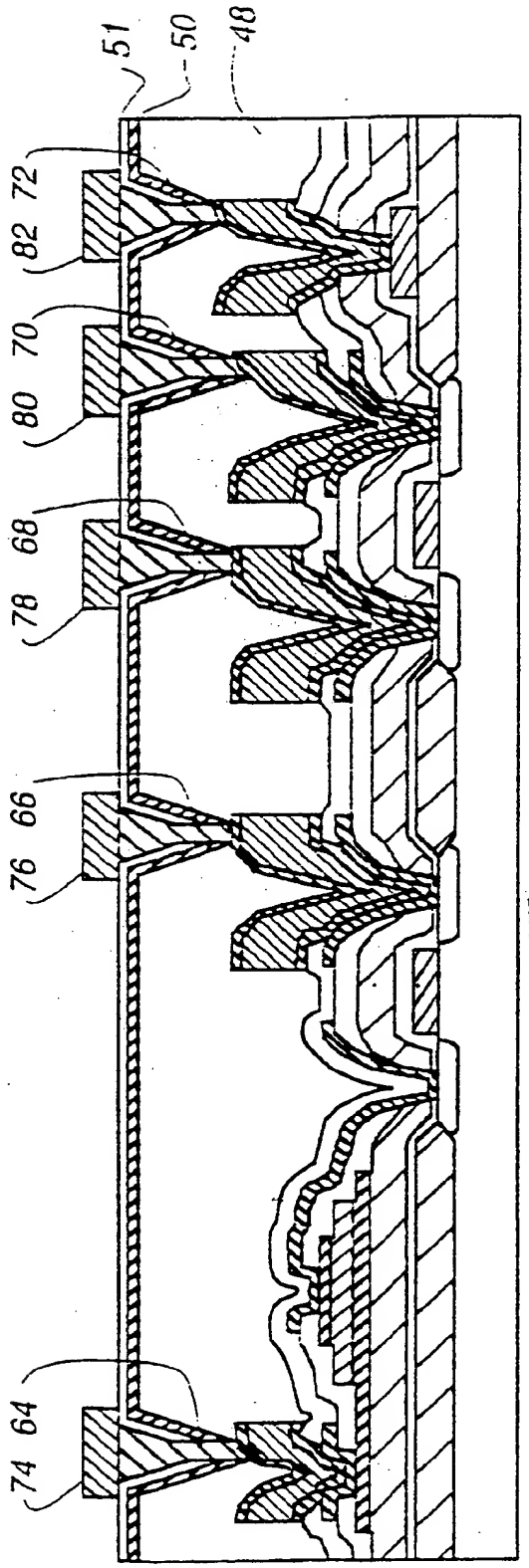
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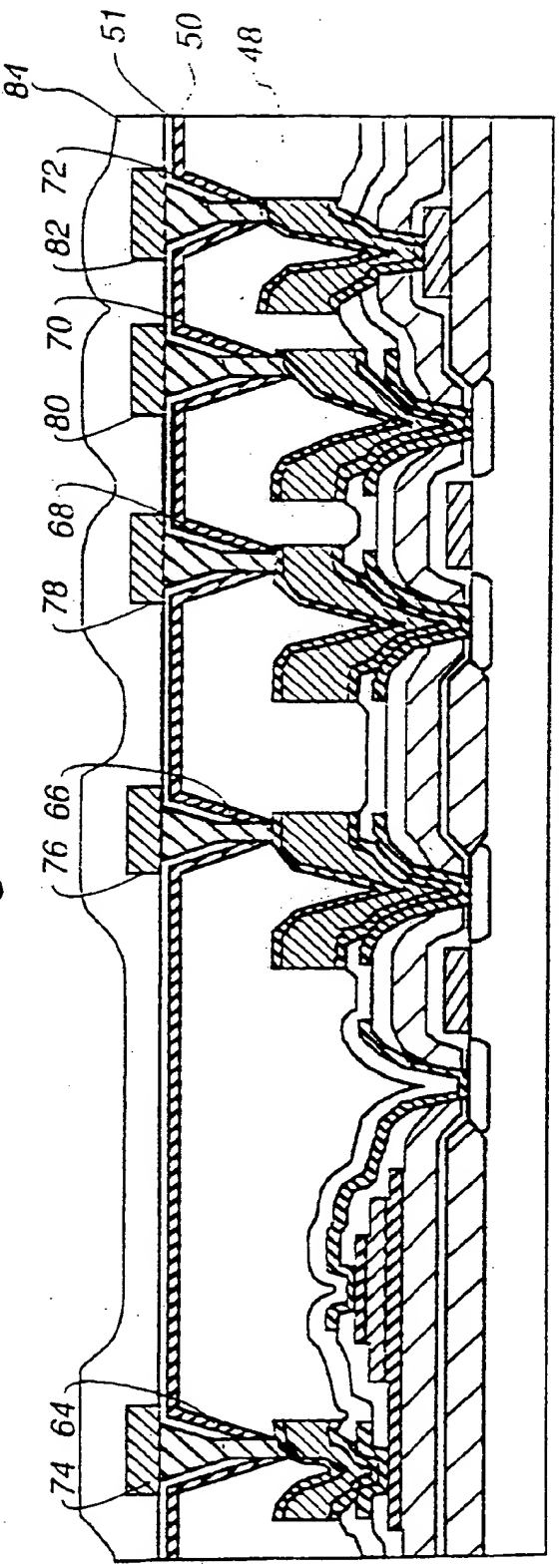
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Fig. 16

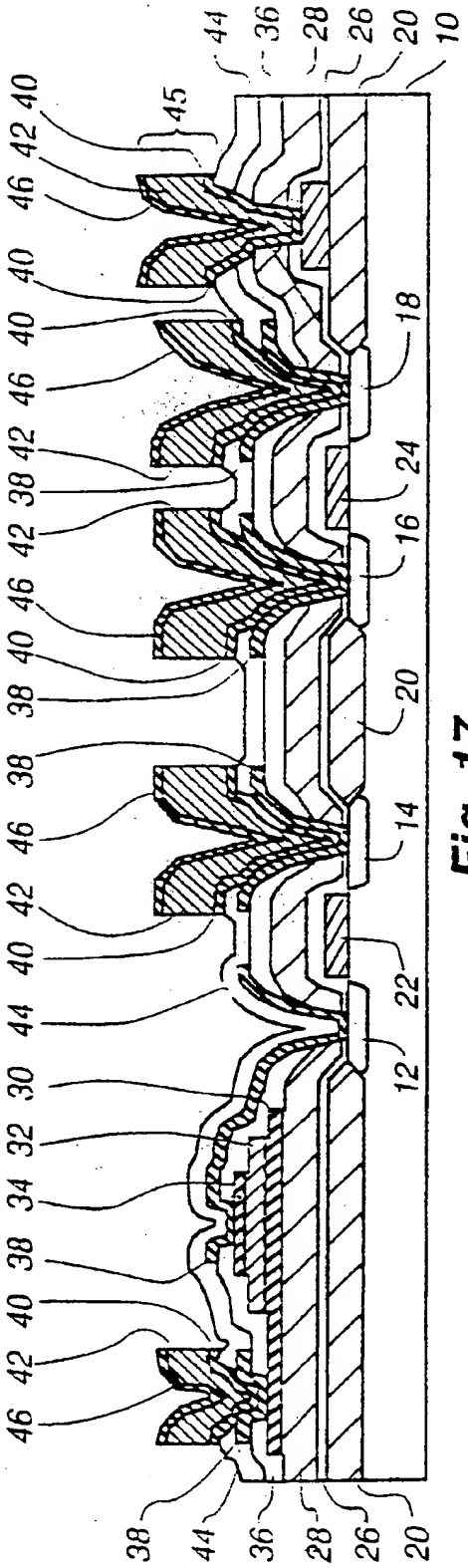
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Fig. 17

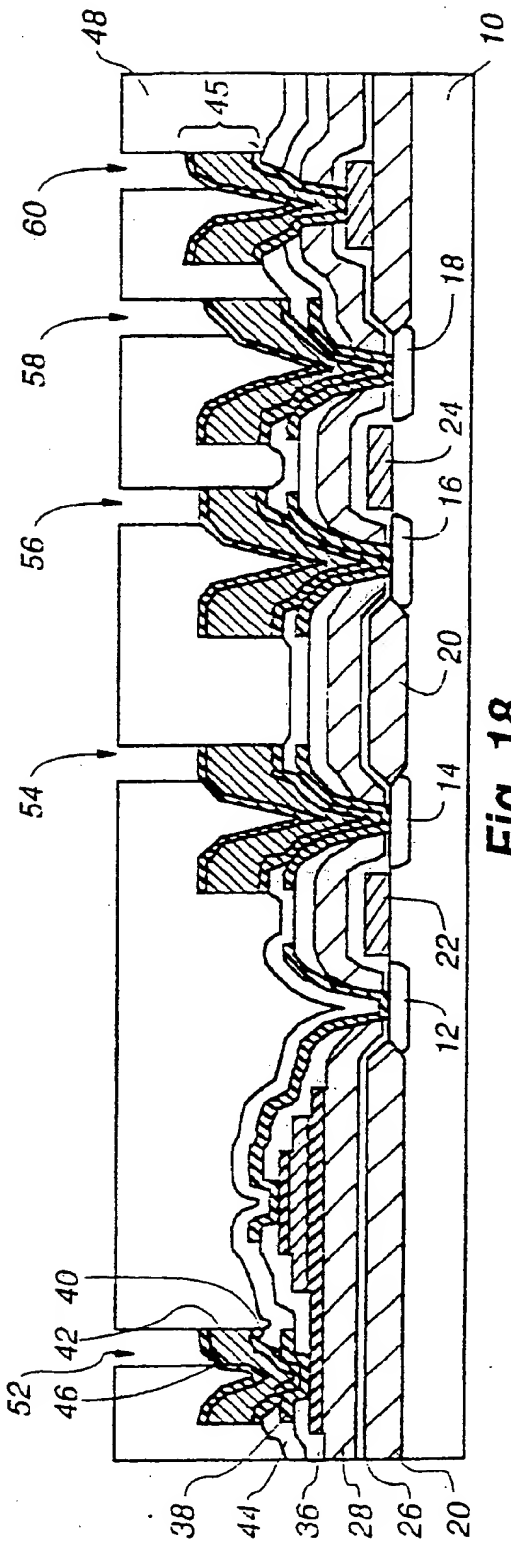
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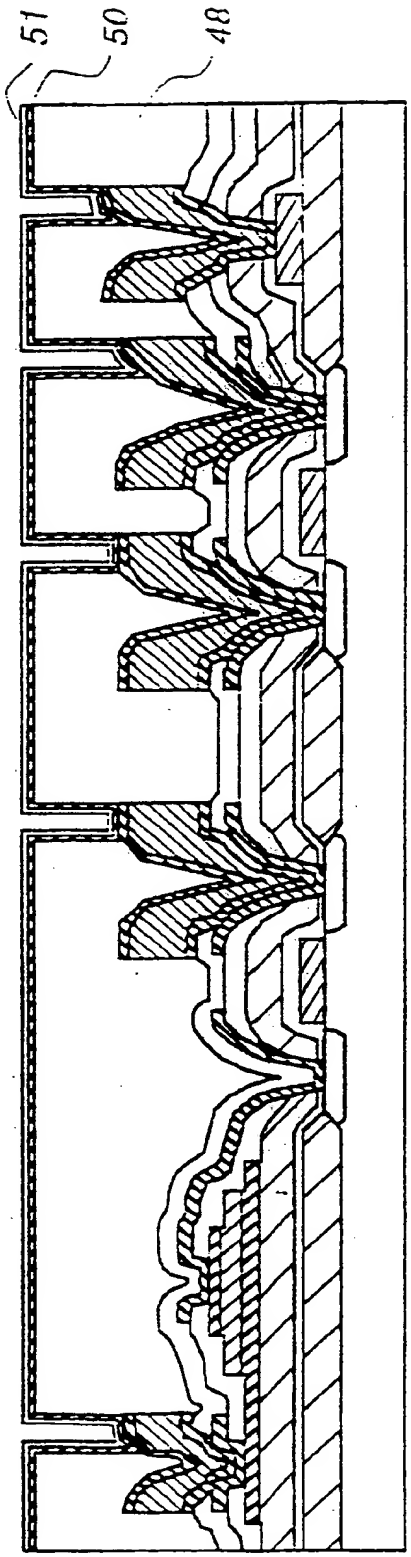
Fig. 18



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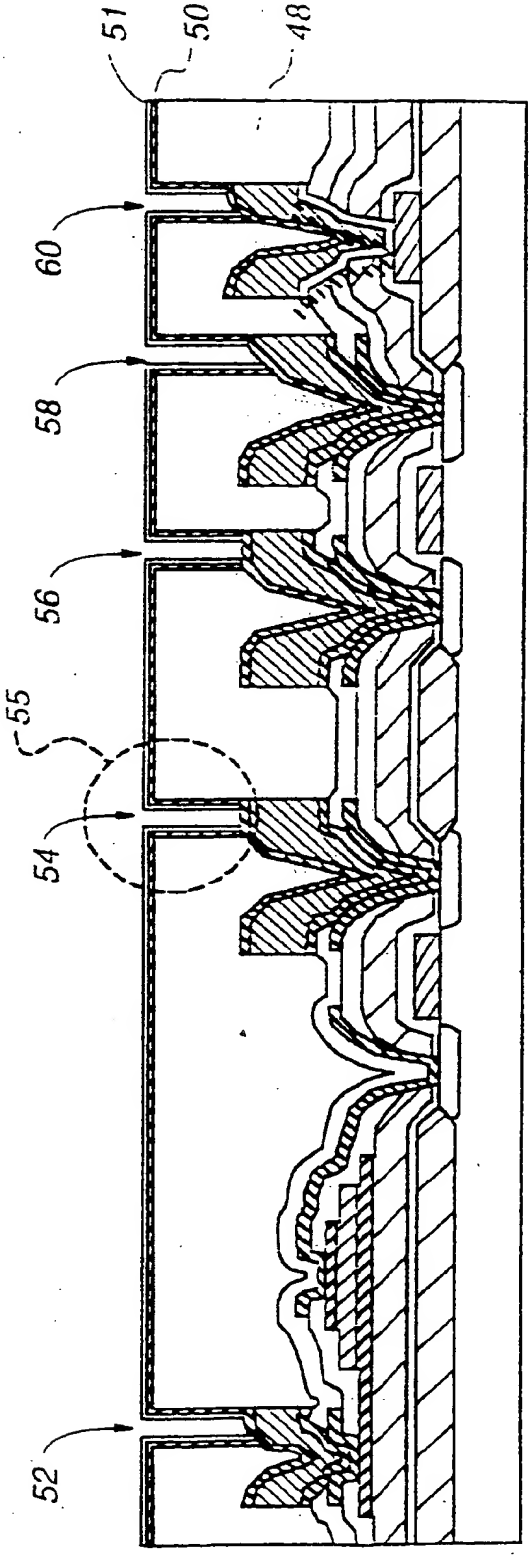

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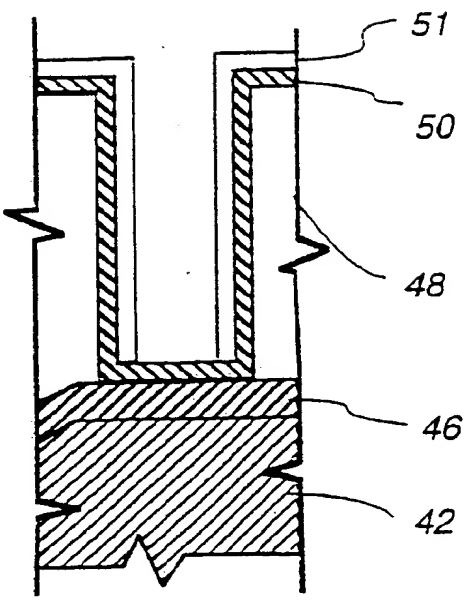


Fig. 20A

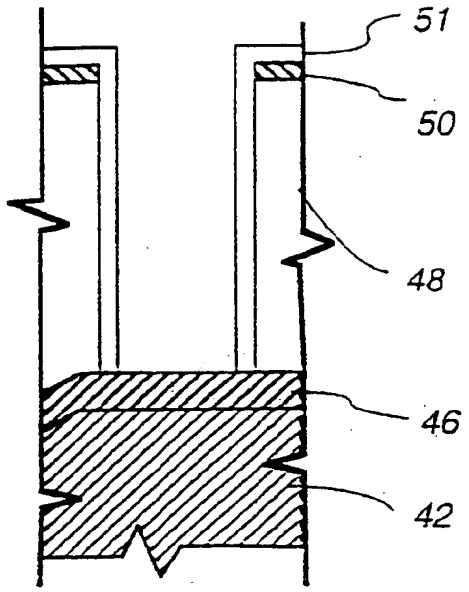


Fig. 20B

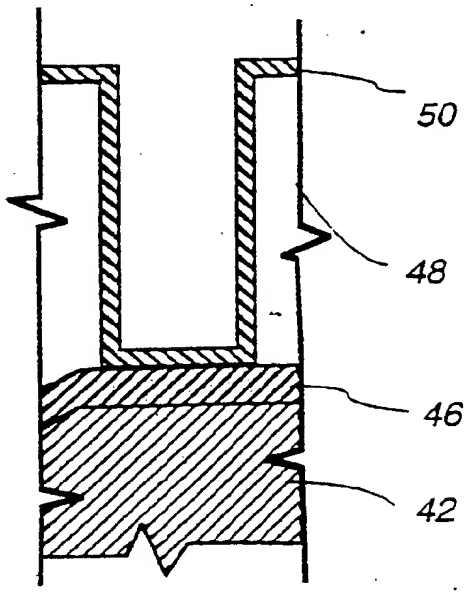


Fig. 20C

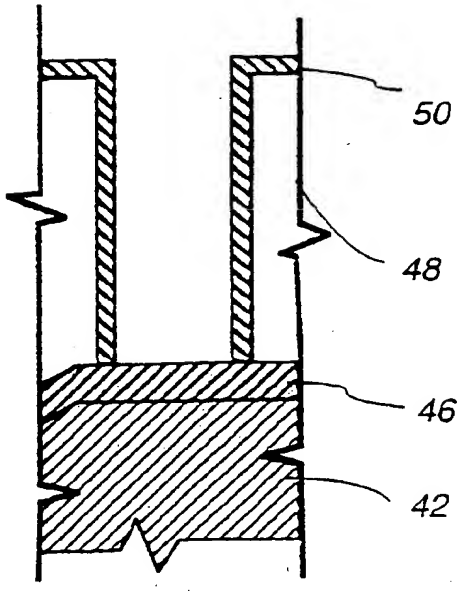
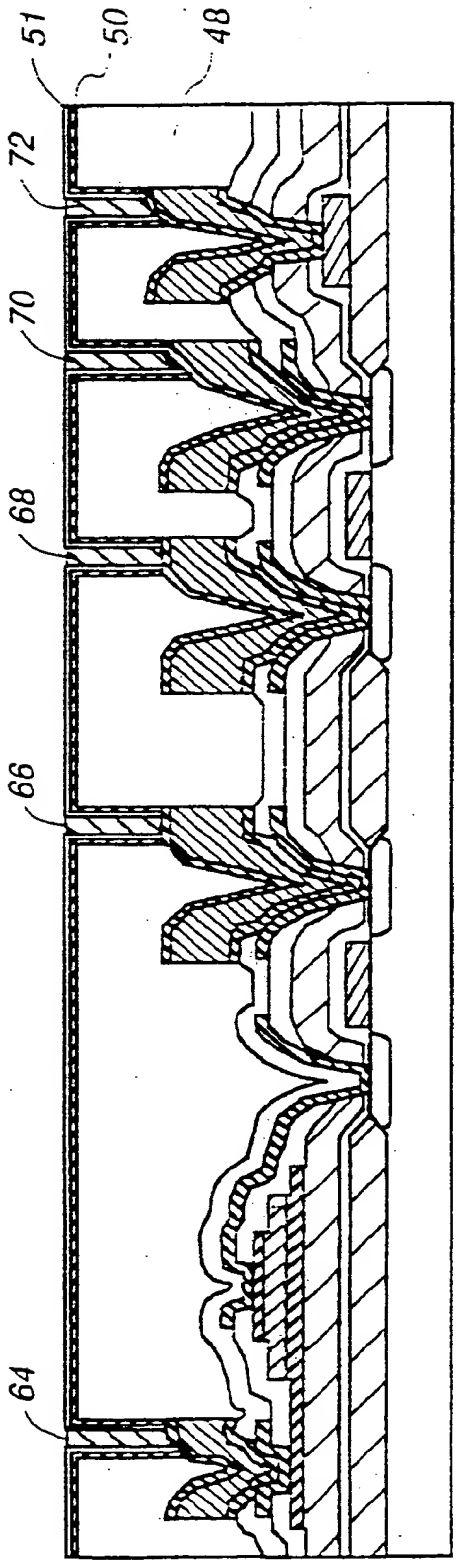


Fig. 20D



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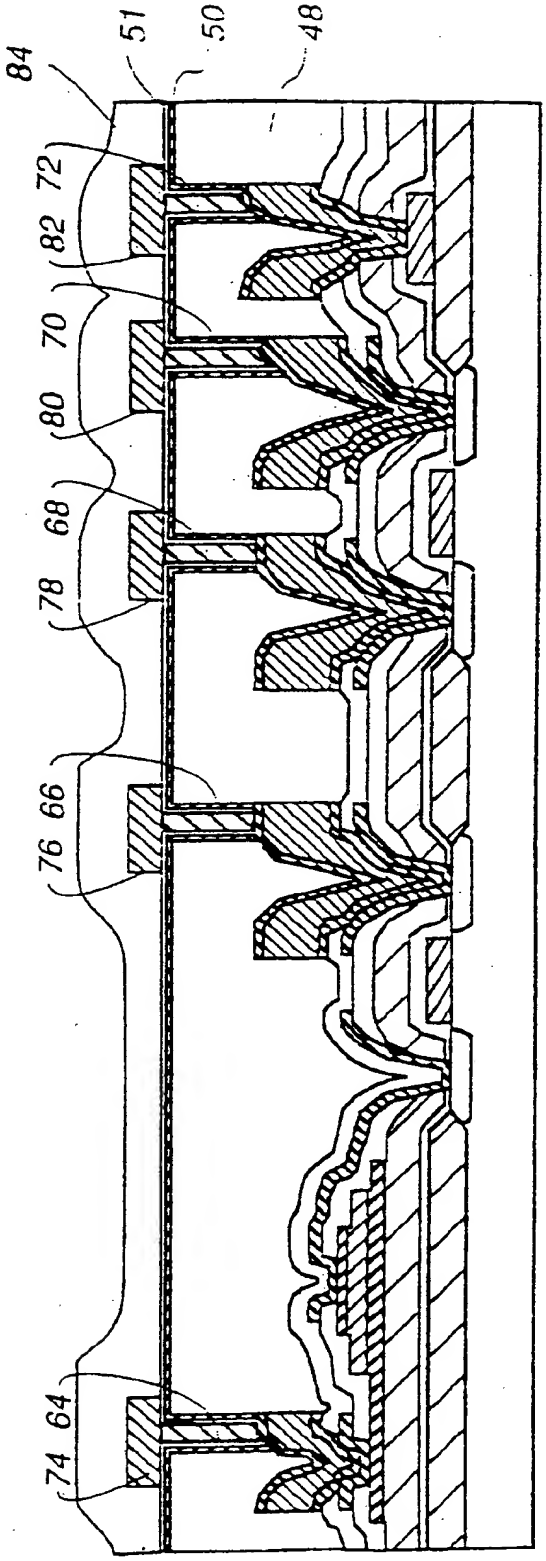


Fig. 22

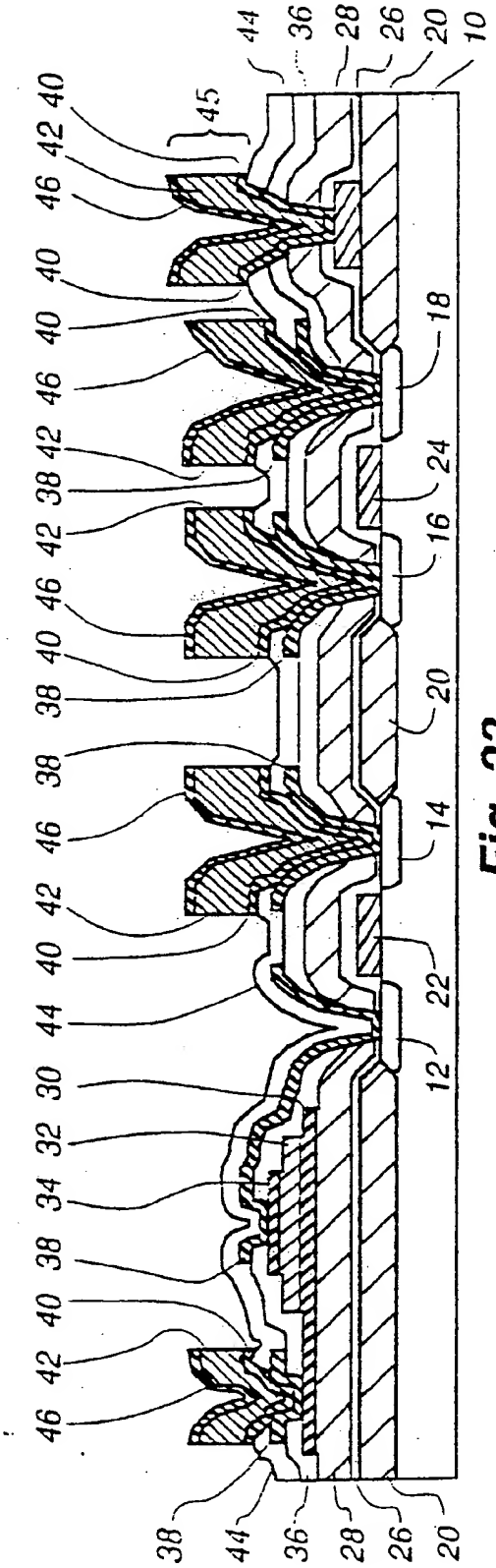
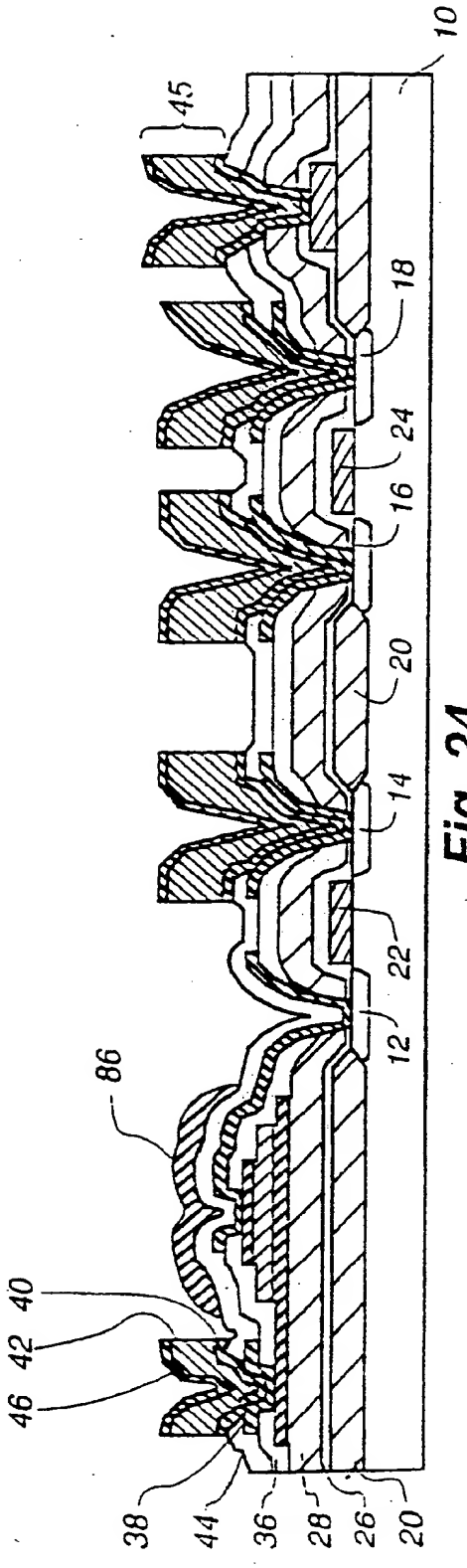


Fig. 23



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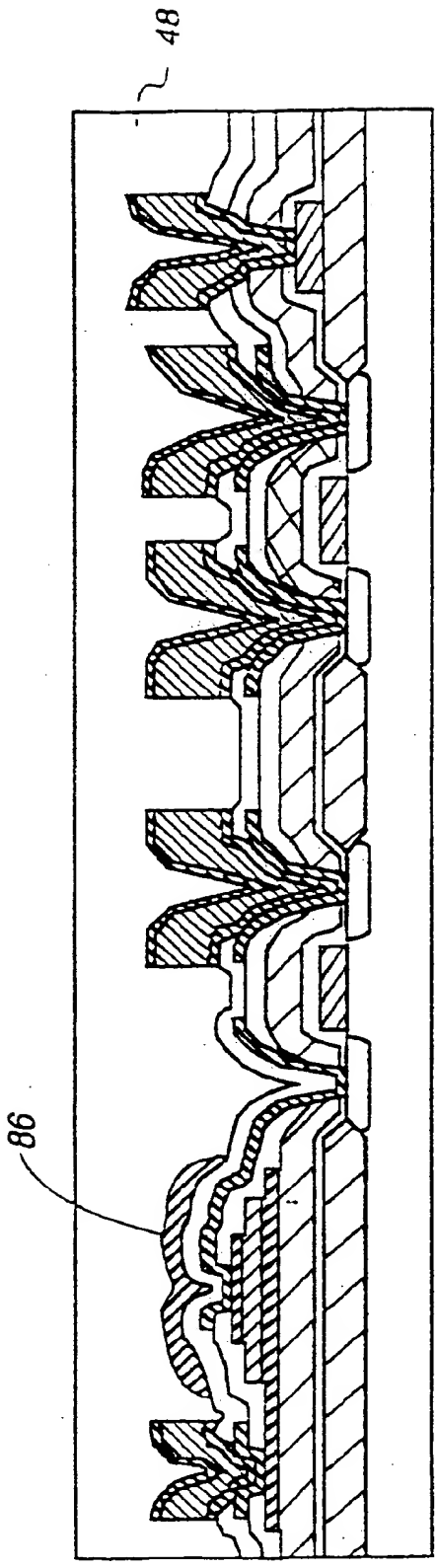

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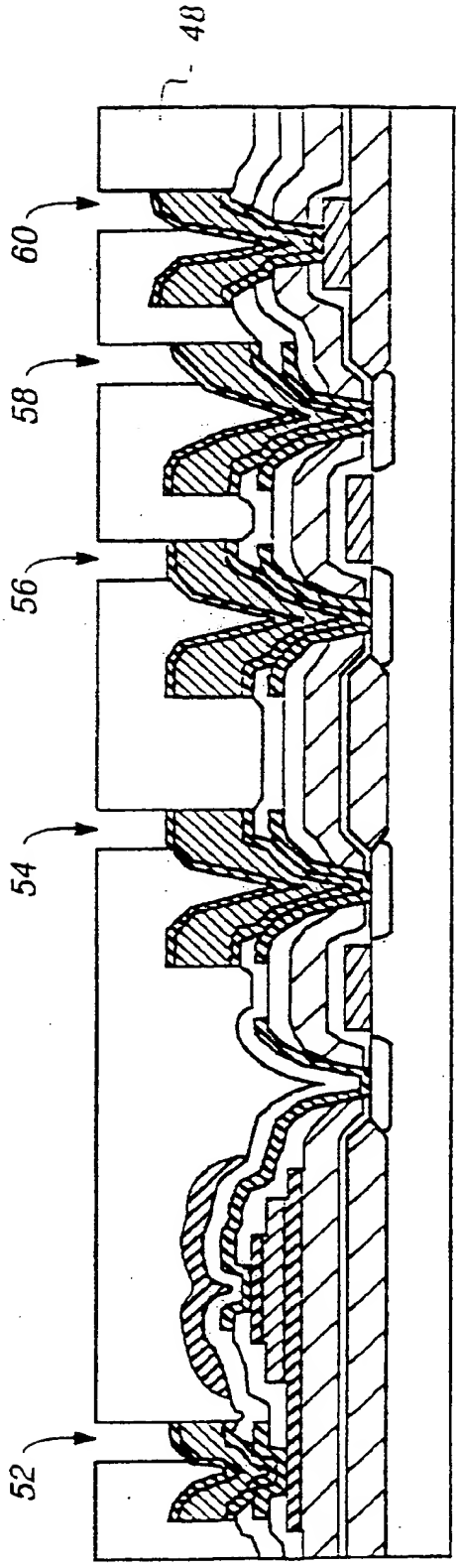

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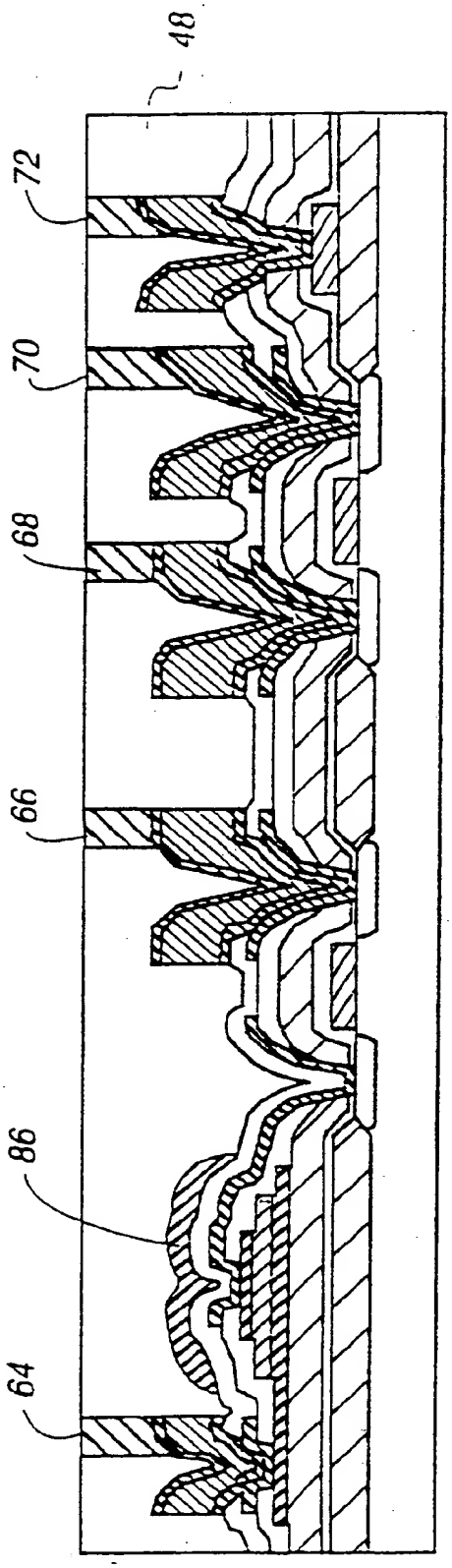

Fig. 27

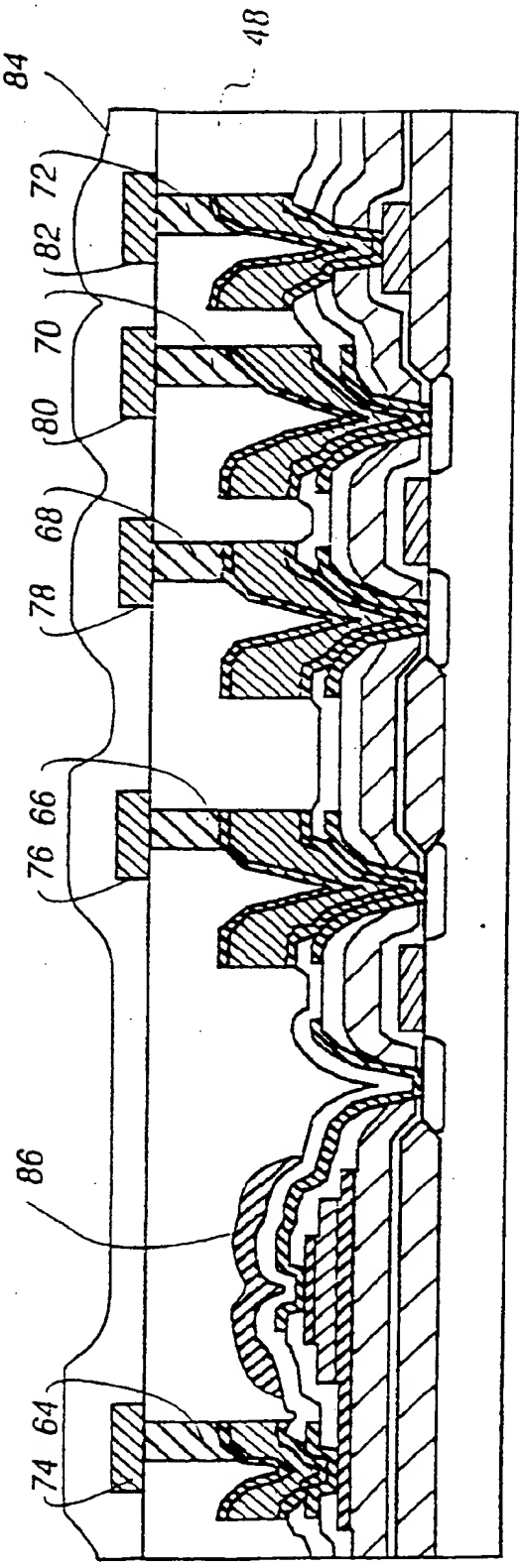

Fig. 28

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 30 2764

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X Y	EP 0 514 547 A (SEIKO EPSON CORP) 25 November 1992 * page 3, column 4, line 12 - page 5, column 7, line 52; figures 1-5E *	1,2,5-9, 12,15, 18,21,22 3,4,10, 11,13, 14,16, 17,19,20	H01L21/8247 H01L21/3205 H01L27/115 H01L23/532 H01L23/00
Y	EP 0 671 765 A (RAMTRON INT CORP) 13 September 1995 * page 4, column 3, line 45 - page 5, column 6, line 47; figures 1-4 *	3,4,10, 11,13, 14,16, 17,19,20	
A	US 5 481 490 A (WATANABE HITOSHI ET AL) 2 January 1996 * column 7, line 25 - column 10, line 12; figures 1-4 *	1,5,7,9, 12,15, 18,21,22	
A A	EP 0 766 319 A (SONY CORP) 2 April 1997 * page 6, line 4 - page 10, line 38; figures 4-6F *	1,2,5,7, 8,12,15, 18,21,22	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 July 1998	Albrecht, C

CATEGORY OF CITED DOCUMENTS

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